

Description

Common Controller Area Network Interface

Technical Field

- [01] This invention relates to the field of computer interfaces, and more specifically, a system to interface an electronic device to a plurality of two-wire and four-wire network standards.

Background

- [02] A number of years ago, the automotive industry was seeking a solution to the problem of the proliferation of wiring in automotive systems as the complexity of automotive controls was increasing. The number of electronic devices having the need to communicate with each other and with a central processor increased dramatically as antilock braking systems and traction controls become commonplace in vehicles. Often, several control devices needed access to the same process inputs, and accessing these inputs individually by the control devices was not practical. To simplify the communication of information among sensors, controllers, and displays, the automotive industry established the Controller Area Network (CAN) for communication of automotive data along a two wire, high speed data bus.
- [03] While CAN is a standard in widespread use, many other similar standards exist. A standard version of CAN is the CAN J-1939 standard designed for heavy trucks and off-highway vehicles. This standard sets forth a two-wire network topology. One of the wires is a CAN_H or CAN high wire and one of the wires is a CAN_L or CAN low wire. To reduce the effects of noise on the communications bus, a CAN network is a differential network that places a dominant bus condition on the network when CAN_H is at least 0.9 volts higher

10058806-013002

than CAN_L. A recessive bus condition is detected on the network when CAN_H is not higher than 0.5 volts above CAN_L. The nominal voltage on the line in the dominant state is 3.5 volts for CAN_H and 1.5 volts for CAN_L. The CAN network should also be galvanically isolated from the various sensors and controllers attached to the network.

[04] Devicenet is a variation on the CAN network that provides for a four-wire communications bus. In addition to the standards described above for the CAN J-1939 standard, the Devicenet provides a Power and a Ground voltage on the additional two wires. A Devicenet must provide at least 500 volts of galvanic isolation in addition to electrical isolation.

[05] ISO J-11783 is a variation of the CAN network that provides for a four-wire communications bus. In addition to the standards described for the J-1939 standard, the J-11783 standard provides reference voltage levels on the additional two wires. The J-11783 standard requires fault tolerance such that if one of the two data wires is opened or grounded, the network will continue to operate.

[06] The J-1939, Devicenet, and ISO J-11783 standards are all passive networks. In other words, the differential voltage between the CAN_H and CAN_L signals will drift towards zero in the recessive state, but is not pulled to zero. In addition, the DC value of the high and low signal may drift anywhere between about one and four volts.

[07] RS-485 is one type of differential network that utilizes an active network. The differential values on the high and low signals are pushed low or pulled high, but the current is limited to keep the voltage in the zero to five volt range. Modbus is one type of RS-485 network that offers galvanic isolation.

[08] Another active differential network is the CAT datalink. In CAT datalink, resistors are used to tie the high/low line to either +5 volts or ground in order to effectuate a complete reversal of voltage when the bus is placed in a recessive state. In other words, instead of merely letting the high and low lines

drift to a common voltage following the transition from a dominant to a recessive state, the CAT datalink actually reverses the differential voltage.

[09] Because each of these differential networks has slightly different requirements, interfaces have generally been built specific to the type of differential network being utilized. For example, CAT datalink interfaces were designed specifically for CAT datalink buses, and J-1939 interfaces were designed for J-1939 buses. However, it is not cost efficient to build interfaces for devices that are specific to each individual network. An interface is needed that can communicate to a number of these devices without manual reconfiguration.

[10] Peter Hanf describes a CAN interface with enhanced fault tolerance in U.S. Patent number 6,115,831, titled "Integrated Circuit for Coupling a Microcontrolled Control Apparatus to a Two-Wire Bus." Hanf discloses a circuit for interfacing to a CAN device that can communicate despite the presence of a bus fault, thus meeting the CAN standard and the J-11783 standard. Upon detection of a bus fault, the circuit generates a fault signal and alters the termination characteristics of the circuit to continue to operate in the presence of a fault. However, while fault tolerance is provided by the circuit, the circuit is not designed to interface with a great variety of bus designs.

Summary of the Invention

[11] Embodiments of the invention provide an electronic interface for connecting to a network. The network places a data stream on a bus high signal and a bus low signal. The interface includes a ground synthesizer, a capacitive isolator, and an edge triggering circuit. The ground synthesizer circuit synthesizes a ground from the bus high signal and bus low signal. The capacitive isolator circuit generates an isolated bus high signal from the bus high signal, and the edge triggering circuit regenerates the data stream into a first reconstructed data stream by comparing the isolated bus high signal with the ground.

10058806-013002

Brief Description of the Drawings

- [12] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention and together with the description, serve to explain the principles of the invention.
- [13] Figure 1 illustrates a block diagram of a circuit for interfacing to two-wire and four-wire networks consistent with an exemplary embodiment of the present invention.
- [14] Figure 2 illustrates a schematic drawing of an input protection circuit consistent with an exemplary embodiment of the present invention.
- [15] Figure 3 illustrates a schematic drawing of a ground synthesis circuit consistent with an exemplary embodiment of the present invention.
- [16] Figure 4 illustrates a schematic drawing of a capacitive isolation circuit consistent with an exemplary embodiment of the present invention.
- [17] Figure 5 illustrates a schematic drawing of an edge triggering circuit consistent with an exemplary embodiment of the present invention.
- [18] Figure 6 illustrates a schematic diagram of a combinatorial data circuit consistent with an exemplary embodiment of the present invention.
- [19] Figure 7 illustrates a schematic diagram of a combinatorial fault circuit consistent with an embodiment of the present invention.
- [20] Figure 8a illustrates a graph of a typical differential input signal as input into an exemplary embodiment of the present invention.
- [21] Figure 8b illustrates a graph of a typical signal output from isolated CAN high in an exemplary embodiment of the present invention.
- [22] Figure 8c illustrates a graph of a typical signal output from isolated CAN low in an exemplary embodiment of the present invention.
- [23] Figure 8d illustrates a graph of the data high output of the edge triggering circuit in an exemplary embodiment of the present invention.

10058806-013002

- [24] Figure 8e illustrates a graph of the data low output of the edge triggering circuit in an exemplary embodiment of the present invention.
- [25] Figure 8f illustrates a graph of the bitstream out of the combinatorial data circuit of an exemplary embodiment of the present invention.
- [26] Figure 9a illustrates a graph of a faulty differential input signal as input into an exemplary embodiment of the present invention.
- [27] Figure 9b illustrates a graph of a faulty signal output from isolated CAN high in an exemplary embodiment of the present invention.
- [28] Figure 9c illustrates a graph of a signal output from isolated CAN low in an exemplary embodiment of the present invention.
- [29] Figures 9d illustrates a graph of the data high output of the edge triggering circuit during a fault in an exemplary embodiment of the present invention.
- [30] Figures 9e illustrates a graph of the data low output of the edge triggering circuit during a fault in an exemplary embodiment of the present invention.
- [31] Figure 9f illustrates a graph of the bitstream out of the combinatorial data circuit during a fault of an exemplary embodiment of the present invention.

Detailed Description

- [32] Reference will now be made in detail to the exemplary embodiments which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts and signals.
- [33] Figure 1 illustrates a block diagram of a circuit for interfacing to two-wire and four-wire networks consistent with an exemplary embodiment of the present invention. A bus high or CAN high signal 100, power 105, ground 110, and a bus low or CAN low signal 115 may be present in a four-wire network bus. In two-wire implementations (e.g., CAT datalink, RS-485, or J-1939),

10058806.013002

power 105 and ground 110 may not be present. In four-wire implementations (e.g., J-11783 or Devicenet), power 105 and ground 110 may actually provide power and ground, respectively, or they may be reference voltage signals, depending on the standard implemented on the bus.

- [34] An optional input protection circuit 117 provides limitations on the amount that a J-11783 or Devicenet implementation will load the bus. The input protection circuit 117 may have current limiting features to prevent current spikes or electrostatic discharge from progressing through the circuitry of the interface. In addition, the input protection circuit 117 may limit the maximum voltage that will be seen by later portions of the circuitry and limits the maximum differential voltage. The input protection circuit 117 also may provide electrical isolation between digital input ground and the chassis ground of the device in which the circuit is located. The input protection circuit 117 provides outputs of protected CAN high 120, ground 125, and protected CAN low 130 to the ground synthesis circuit 132.

- [35] Ground synthesis circuit 132 generates a synthesized ground for two-wire applications that typically do not have the ground wire 110 that is found in most four wire bus implementations. Ground synthesis circuit 132 provides a synthesized ground by averaging the input of the differential signal on protected CAN high 120 and protected CAN low 130. The ground synthesis circuit 132 provides a protected CAN high 135, synthesized high ground 140, synthesized low ground 145, and protected CAN low 150 to capacitive isolation circuit 152.

- [36] Capacitive isolation circuit 152 serves to limit current passing through the circuit and eliminate DC aspects of the signals, such that only AC components of the signals pass through the circuit 152. In other words, only transitions, or edges, of the incoming high and low data signals are transmitted through the capacitive isolation circuit 152. The capacitive isolation circuit 152 provides an isolated CAN high 155, an isolated high ground 160, an isolated low

1056306-013002

ground 165, and an isolated CAN low 170 signal to the edge triggering circuit 172.

[37] Edge triggering circuit 172 provides data high and data low signals to combinatorial and fault logic for processing. The edge triggering circuit incorporates schmitt triggering features to reduce noise sensitivity. The incoming CAN signals to the input protection circuit 117 may be noisy, experiencing various ESD and RF noise. Edge triggering circuit 172 contains circuitry to take the incoming AC edge signals and reconstruct DC logic level signals. The edge triggering circuit sends data high 182 and data low 178 signals to the combinatorial data circuit 186. In addition, the edge triggering circuit sends data low pump 175 and data high pump 177 to the combinatorial fault circuit 190.

[38] Combinatorial data circuit 186 takes the two individual pulse trains, data high 182 and data low 178, and generates a single bit stream of data 188. During non-fault operation of the system, the bitstream will mirror the data high 182 input. The combinatorial data circuit 186 will continue to generate an accurate bitstream even upon the loss of one of the two input signals when a low ground and/or high ground signal is present.

[39] Combinatorial fault circuit 190 takes input signals from the edge triggering circuit 172 and generates a fault signal 192 if one or both input data streams are absent.

[40] A detailed discussion of exemplary circuits will now be discussed. Figure 2 illustrates a schematic drawing of an input protection circuit 117 consistent with an exemplary embodiment of the present invention. Resistors 220, 225 and 235 are current limiting resistors to provide protection to the remainder of the circuitry from incoming spikes. As discussed previously, these data buses are often operated in electrically noisy environments.

[41] Resistor 225 and capacitor 230 are utilized to limit the loads on the power lines of a four-wire bus to remain within the specified load limit of the

bus standards. Series diode pairs 240 and 250 take an incoming low signal and shunt an incoming low level signal to datalink ground (indicated by the darkened ground symbol 205); the diode pairs 240 and 250 also function to take a high level signal and shunt it to the high side of zener diode 260. In the exemplary embodiment of the invention, zener diode 260 is a 12 volt zener. Thus, the series diode pairs 240 and 250 drive a low incoming signal to ground and a high incoming signal to approximately 12 volts.

[42] The zener diode 260, along with diode pairs 240 and 250, prevent the incoming differential signal on CAN high 100 and CAN low 115 from having a differential voltage of greater than the zener diode's value, e.g., in the exemplary embodiment 12 volts. Zener diodes 265, 270, and 275 provide operating margin between the datalink ground and chassis ground. Additional zener diodes may be used to provide operating margin between chassis ground and internal circuitry ground (shown in the drawings as a non-filled ground).

[43] Figure 3 illustrates a schematic drawing of the ground synthesis circuit 132 consistent with an exemplary embodiment of the present invention. Resistor bridges 305, 310, and 315 are utilized to either use the incoming ground signal 125 or, if the incoming ground signal is not present, generate a synthesized ground. In an exemplary embodiment of the present invention, resistors 310 and 315 are equivalently sized such that they equally divide the voltage differential between protected CAN high 120 and protected CAN low 130 to generate the synthesized ground output as synthesized high ground 140 and synthesized low ground 145. Therefore, regardless of what is connected, a ground, at some appropriate DC or AC voltage level, will be generated.

[44] Figure 4 illustrates a schematic drawing of the capacitive isolation circuit 152 consistent with an exemplary embodiment of the present invention. Capacitors 405, 410, 420, and 425 remove the DC component of the incoming signals, sending only edges of the signal through the capacitive isolation circuit

10058806-013002

152. Resistors 430, 435, 440, and 445 are in place to further serve as current limiters.

[45] Figure 5 illustrates a schematic drawing of the edge triggering circuit 172 consistent with an exemplary embodiment of the present invention. The edge triggering circuit 172 receives an isolated CAN high 155, an isolated high ground 160, an isolated low ground 165, and an isolated CAN low 170 signal from the capacitive isolation circuit 152. The isolated high ground 160 and isolated low ground 165 signals should be relatively steady signals, with the exception of any noise that appears from operation of the bus. The isolated CAN high 155 will provide a positive pulse on a high transition of CAN high 100 to a dominant state and will provide a negative pulse on a low transition of CAN high 100 to a recessive state. The isolated CAN low 170 will provide a negative pulse on a low transition of CAN low 115 to a dominant state and will provide a positive pulse on a high transition of CAN low 115 to a recessive state. Kicking circuits 525, 530, 540, and 542 provide a DC bias to provide the voltage bias for the pulses and bias the differential amplifier circuitry 509.

[46] A data high differential amplifier 511 includes transistors 506, 508, and 510. On a positive spike from isolated CAN high 155, transistor 508 will turn on and transistor 506 will turn off. This will turn on transistor 555, which will supply power through schottky diode 504, giving schmitt trigger feedback to latch the data high differential amplifier 511 in an on state. On a negative spike from isolated CAN high 155, transistor 508 will turn off and transistor 506 will turn on. This will turn off transistor 555, which will provide schmitt trigger feedback through schottky diode 502 to hold the data high differential amplifier 511 in the off state. The use of schmitt triggers provides a fast turn off and turn on time, in addition to hysteresis useful in meeting various standards and rejecting signal noise. Thus, a reconstructed data stream is regenerated from the incoming pulse stream. This signal is output on data high 182 for use in the combinatorial data circuit 186. In addition, a data high pump

signal 177 of discrete data is sent to the combinatorial fault circuit 190 for monitoring fault detection.

- [47] A data low differential amplifier 517 includes transistors 512, 514, and 516. The data low differential amplifier 517 functions analogously to the data high differential amplifier 511, except with reverse polarity. It outputs a clean data low 178 signal for use in combinatorial data circuit 186. In addition, a data low pump 175 signal is used in the combinatorial fault circuit 190 for monitoring fault detection.

- [48] Figure 6 illustrates a schematic diagram of a combinatorial data circuit 186 consistent with an exemplary embodiment of the present invention. Capacitors 602 and 603 take the incoming data high 182 signal and data low 178 signal, respectively, and transform the digital square wave input signal into a series of pulses, similar to the operation of the capacitive isolation circuit 152. This provides a data high pulse train and a data low pulse train to the differential amplifier that includes transistors 605, 610 and 615. Kicking circuits 635 and 640 provide a DC bias to provide the voltage bias for the pulses and bias the differential amplifier circuitry. The differential amplifier operates in conjunction with the schottky diodes 620 and 625 and transistor 670 to turn the pulses back into a square wave.

- [49] Assuming both signal lines are operational, in other words there are transitions occurring on both data high 182 and data low 178, the differential amplifier should see a pair of opposite pulses on its inputs. When a dominant state is placed on the bus, the differential amplifier should see a positive pulse out of the capacitor on the data high 182 line and a negative pulse out of the capacitor on the data low 178 line. The differential amplifier will then latch in an ON state. When a recessive state is placed on the bus, the differential amplifier should see a negative pulse out of the capacitor on the data high 182 line and a positive pulse out of the capacitor on the data low 178 line. Thus the differential amplifier should latch in an OFF state.

[50] If one of the pulse trains is missing, due to an open or shorted input line for instance, the differential amplifier will continue to operate. For instance, if no signal is present on the data low 178 input, on a transition to a dominant state the output of capacitor 602 will be a positive pulse. There will be no pulse out of the capacitor 603 from the data low 178 input. However, there will still be enough positive differential voltage present when comparing the pulse on the high side to the low voltage on the low side to switch the state of the differential amplifier. Thus, a bit stream will always be present on bitstream 188, so long as one of the two differential input lines is working.

[51] Figure 7 illustrates a schematic diagram of the combinatorial fault circuit 190 consistent with an exemplary embodiment of the present invention. The combinatorial fault circuit 190 uses two charge capacitors 730 and 735 to keep MOSFETS 740 and 745 turned on as long as a pulse stream is present on both differential input lines. When these MOSFETS 740 and 745 are turned on, fault signal 192 remains low (false), but should either pulse stream become inactive, the associated MOSFET 740 and/or 745 will turn off, placing a high signal on the fault signal 192.

[52] Data low pump 175 and data high pump 177 feed a signal into buffers 710 and 715, respectively. Buffers 710 and 715 act as a high impedance buffer so as to not load down transistors 550 and 555. Pump circuits 720 and 725 act to charge up charge capacitors 730 and 735 as long as data is coming in to data low pump 175 and data high pump 177. For instance, when the data signal is high at buffer 710, pump circuit 720 powers up the capacitor through the lower diode, and when the data signal is low at buffer 710, pump circuit 720 discharges through the upper diode to keep capacitor 730 charged up. Any overcharging is bled off to the supply voltage. Resistors 732 and 737 in parallel to the charge capacitors 730 and 735 provide enough of a time constant to not bleed off the charge capacitors 730 and 735 if there is a momentary blip in the input signal. If the signal is lost past the time delay of the time constant, the charge capacitors

10058806-013002

discharge thereby turning off MOSFETS 740 or 745. This provides a fault indication on fault signal 192.

- [53] Those skilled in the art will appreciate that while discrete components are illustrated in this exemplary embodiment, integrated circuit construction is also contemplated. Each component in this description, or an equivalent thereof, can be implemented in an integrated circuit, and such construction would be considered to be at least an equivalent of the above described circuitry. In addition, those skilled in the art will appreciate that transistor type, e.g., PNP/NPN, NFET, PFET or BJT can be substituted with appropriate changes in circuitry to achieve similar results. In addition, while discrete transistors are shown, differential amplifiers can also be constructed from operational amplifiers meeting the necessary speed requirements and propagation delay to function at CAN data speeds.

- [54] Figures 8a-8f illustrate a time domain graph of differential voltage signals during normal operation in the circuit of an exemplary embodiment of the present invention. Figures 9a-9f illustrate a time domain graph of differential voltage signals in the circuit during a fault of an exemplary embodiment of the present invention. These figures will be discussed more fully in the following Industrial Applicability portion of this specification.

Industrial Applicability

- [55] Figure 8a illustrates a typical differential input signal as input into an exemplary embodiment of the present invention. A CAN high input 805 is input at CAN high input 100. A CAN low input 810 is input at CAN low input 115. In a recessive state, prior to time $t=1$, between times $t=2$ and $t=3$, and after time $t=4$, the two inputs float at a similar voltage. At time $t=1$, a dominant state is placed on the bus and a differential voltage is placed across the inputs. This differential voltage remains until time $t=2$ when the differential voltage is removed and the two inputs return to a similar voltage.

10058806-013002

- [56] Figures 8b and 8c illustrate a graph of the output of the capacitive isolation circuit in an exemplary embodiment of the present invention. Figure 8b illustrates a typical signal output from isolated CAN high 155, and Figure 8c illustrates a typical signal output from isolated CAN low 170.
- [57] On the high side of the differential input, as the input signal 805 goes high at time $t=1$, the capacitive isolation circuit 152 removes the DC component from the signal and provides a positive pulse. At time $t=2$, the capacitive isolation circuit 152 provides a negative pulse. These pulses are provided on isolated CAN high 155 to the edge triggering circuit 172.
- [58] On the low side of the differential input, as the input signal 810 goes low at time $t=1$, the capacitive isolation circuit 152 removes the DC component from the signal and provides a negative pulse. At time $t=2$, the capacitive isolation circuit 152 provides a positive pulse. These pulses are provided on isolated CAN low 170 to the edge triggering circuit 172.
- [59] Figures 8d and 8e illustrate a graph of the output of the edge triggering circuit 172 in an exemplary embodiment of the present invention. Through operation of the differential amplifiers, transistors, and schmitt triggers, the edge triggering circuit 172 reconstructs a digital data signal from the incoming pulses. At time $t=1$, a positive pulse arrives on the high side, thus turning on the high side differential amplifier. A negative pulse also arrives on the low side, thus turning off the low side differential amplifier. At time $t=2$, opposite pulses arrive reversing the latching of the differential amplifiers.
- [60] Figure 8f illustrates a graph of the bitstream out of the combinatorial data circuit 186 of an exemplary embodiment of the present invention. The combinatorial data circuit 186 reconverts the signal back into pulses and then compares the high data and low data stream to generate an output bitstream. The output bitstream in the graph is the same as the graph illustrated in Figure 8d because both inputs are intact.

[61] Figure 9a illustrates a faulty differential input signal as input into an exemplary embodiment of the present invention. A CAN high input 905 would be input at CAN high input 100. A CAN low input 910 would be input at CAN low input 115. In a recessive state, prior to time $t=1$, the two inputs float at a similar voltage. At time $t=1$, a dominant state is placed on the bus and a differential voltage is placed across the inputs. This differential voltage remains until time $t=2$ when the differential voltage is removed and the two inputs should return to a similar voltage. However, the high side of the bus has grounded at approximately time $t=2$. Thus, only the low side of the differential input is functional after this point.

[62] Figures 9b and 9c illustrate a graph of the output of the capacitive isolation circuit during a fault in an exemplary embodiment of the present invention. Figure 9b illustrates a faulty signal output from isolated CAN high 155, and Figure 9c illustrates a typical signal output from isolated CAN low 170.

[63] On the high side of the differential input, as the input signal 905 goes high at time $t=1$, the capacitive isolation circuit 152 removes the DC component from the signal and provides a positive pulse. At time $t=2$, the capacitive isolation circuit 152 provides a negative pulse. These pulses are provided on isolated CAN high 155 to the edge triggering circuit 172. However, after time $t=2$, the high side of the input CAN is grounded, so no further pulses are generated.

[64] On the low side of the differential input, as the input signal 910 goes low at time $t=1$, the capacitive isolation circuit 152 removes the DC component from the signal and provides a negative pulse. At time $t=2$, the capacitive isolation circuit 152 provides a positive pulse. These pulses are provided on isolated CAN low 170 to the edge triggering circuit 172.

[65] Figures 9d and 9e illustrate a graph of the output of the edge triggering circuit 172 during a fault in an exemplary embodiment of the present invention. Through operation of the differential amplifiers, transistors, and schmitt triggers, the edge triggering circuit 172 reconstructs a digital data signal from the

incoming pulses. At time $t=1$, a positive pulse arrives on the high side, thus turning on the high side differential amplifier. A negative pulse also arrives on the low side, thus turning off the low side differential amplifier. At time $t=2$, opposite pulses arrive, thereby reversing the latching of the differential amplifiers. However, after time $t=2$, no further pulses are received by the high side differential amplifier, so the differential amplifier remains in the off state and no further data is output from the high side.

[66] Figure 9f illustrates a graph of the bitstream out of the combinatorial data circuit 186 during a fault of an exemplary embodiment of the present invention. The combinatorial data circuit 186 reconverts the signal back into pulses and then compares the high data and low data stream to generate an output bitstream. The output bitstream in the graph turns on at time $t=1$ because the high side input is greater than the low side input. At time $t=2$, the output reverses as the high side input falls and the low side input rises. At time $t=3$, there are no pulses generated by the high side to the differential amplifier because of the loss of signal. However, pulses remain coming from the low side, thus continuing to latch the differential amplifier on and off as the low side input changes. Thus, a failure of one of the two differential inputs continues to drive the system successfully.

[67] The disclosed system may act to interface an electronic device to a plurality of two-wire and four-wire network standards. This interface can be accomplished without manual reconfiguration. Because the interface is not specific to a single network, cost efficiencies can be obtained in implementing the system.

[68] It will be readily apparent to those skilled in this art that various changes and modifications of an obvious nature may be made, and all such changes and modifications are considered to fall within the scope of the appended claims. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed

10058806.013002

herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims and their equivalents.

10558806.013002